In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Original) A printed circuit board having a surface providing a mating interface to which is electrically connected an electrical connector having signal conductors and ground conductors, the printed circuit board comprising:

a plurality of stacked dielectric layers, with a conductor disposed on at least one of the plurality of dielectric layers;

the mating interface including:

a plurality of conductive vias aligned in a plurality of rows, the plurality of conductive vias extending through at least a portion of the plurality of dielectric layers, at least one of the plurality of conductive vias intersecting the conductor;

the plurality of conductive vias including signal conductor connecting conductive vias and ground conductor connecting conductive vias; and

for each of the plurality of rows of the conductive vias, there are at least twice as many ground conductor connecting conductive vias as signal conductor connecting conductive vias and the conductive vias are positioned relative to one another so that for each signal conductor connecting conductive via, there are ground conductor connecting conductive vias adjacent either side of the signal conductor connecting conductive via.

2. (Original) The printed circuit board of claim 1, wherein a distance between a signal conductor connecting conductive via and an adjacent ground conductor connecting conductive via of a row is less than a distance between adjacent rows of the conductive vias.

3. (Original) The printed circuit board of claim 1, wherein for each of the plurality of rows of the conductive vias, a distance between a signal conductor connecting conductive via and an adjacent ground conductor connecting conductive via on one side is similar to a distance between the signal conductor connecting conductive via and an adjacent ground conductor connecting conductive via on the other side.

4. (Original) The printed circuit board of claim 1, which further comprises a surface mounting pad disposed on each of the plurality of conductive vias, the signal conductors and ground conductors of the electrical connector being electrically connected to the surface mounting pads.

5. (Original) The printed circuit board of claim 4, wherein the surface mounting pad corresponding to each signal conductor connecting conductive via is substantially configured in an I-shape and the surface mounting pads corresponding to adjacent ground conductor connecting conductive vias are substantially configured in an H-shape.

6. (Original) The printed circuit board of claim 1, which further comprises:

a ground plane layer through which at least some of the plurality of conductive vias extend; and

for each signal conductor connecting conductive via of the ground plane layer, there is provided an area surrounding the signal conductor connecting conductive via that is free of the ground plane layer.

7. (Original) The printed circuit board of claim 6, wherein for each ground conductor connecting conductive via of the ground plane layer, there is provided at least one discrete area adjacent the ground conductor connecting conductive via that is free of the ground plane layer.

8. (Original) The printed circuit board of claim 1, which further comprises:

a power voltage plane layer through which at least some of the plurality of conductive vias extend; and

for each signal conductor connecting conductive via and its corresponding adjacent ground conductor connecting conductive vias extending through the power voltage plane layer, there is provided an area surrounding the conductive vias that is free of the power voltage plane layer.

9. (Currently amended) A printed circuit board having a surface providing a mating interface to which is electrically connected an electrical connector having signal conductors and ground conductors, each signal conductor having a contact tail, with the signal conductor contact tails disposed in a plurality of rows of signal conductor contact tails, and each ground conductor having at least one pair of contact tails positioned along a row of the plurality of rows of signal conductor contact tails, with each signal conductor contact tail being positioned between ground conductor contact tails of a pair, the printed circuit board comprising:

a plurality of stacked dielectric layers;

the mating interface including:

a plurality of conductive ~~vias~~ pads aligned in a plurality of rows of conductive pads~~, the plurality of conductive vias extending through at least a portion of the plurality of dielectric layers~~;

the plurality of conductive ~~vias~~ pads including signal conductor ~~connecting~~ conductive ~~vias~~pads and ground conductor connecting conductive ~~vias~~pads; and

for each of the plurality of rows of the conductive ~~vias~~pads, each signal conductor ~~connecting~~ conductive ~~via~~pad has corresponding ground conductor ~~connecting~~ conductive ~~vias~~pads adjacent either side of the signal conductor ~~connecting~~ conductive ~~via~~pad so as to form a repeating pattern along the row of ground conductor connecting conductive ~~via~~pad – signal conductor ~~connecting~~ conductive ~~via~~pad – ground conductor ~~connecting~~ conductive ~~via.~~pad; and

wherein each signal conductor contact tail aligns with a signal conductor conductive pad and each ground conductor contact tail aligns with a ground conductor conductive pad.

10. (Currently amended) The printed circuit board of claim 9, further comprising a plurality of signal conductor connecting conductive vias, each signal conductor connecting conductive via being coupled to a signal conductor conductive pad of the plurality of conductive pads and a plurality of ground conductor conductive connecting vias, each ground conductor conductive connecting via being coupled to a ground conductor conductive pad of the plurality of conductive pads; and

wherein a distance between a signal conductor connecting conductive via and an adjacent ground conductor connecting conductive via coupled to conductive pads in the same~~of a~~ row of the plurality of rows of conductive pads is less than a distance between signal conductor connecting conductive vias coupled to conductive pads in adjacent rows of the ~~conductive vias~~ plurality of rows of conductive pads.

11. (Currently amended) The printed circuit board of claim ~~9~~10, wherein the plurality of signal conductor connecting conductive vias are disposed in rows and for each of the plurality of rows of ~~the~~signal conductor connecting conductive vias, a distance between a signal conductor connecting conductive via and an adjacent ground conductor connecting conductive via on one side is similar to a distance between the signal conductor connecting conductive via and an adjacent ground conductor connecting conductive via on the other side.

12. (Currently amended) The printed circuit board of claim ~~9~~10, ~~which further~~wherein each of the plurality of conductive pads comprises a surface mounting pad and the printed circuit board comprises a plurality of conductive vias, each disposed below a surface mount pad~~on each of the plurality of conductive vias, the signal conductors and ground conductors of the electrical connector being electrically connected to the surface mounting pads~~.

13. (Original) The printed circuit board of claim 12, wherein the surface mounting pad corresponding to each signal conductor connecting conductive via is substantially configured in an I-shape and the surface mounting pads corresponding to adjacent ground conductor connecting conductive vias are substantially configured in an H-shape.

14. (Currently amended) The printed circuit board of claim 9, further comprising a plurality of signal conductor connecting conductive vias, each signal conductor connecting conductive via being coupled to a signal conductor conductive pad of the plurality of conductive pads and a plurality of ground conductor conductive connecting vias, each ground conductor conductive connecting via being coupled to a ground conductor conductive pad of the plurality of conductive pads; and which further comprises:

a ground plane layer through which at least some of the plurality of conductive vias extend; and

for each signal conductor connecting conductive via of the ground plane layer, there is provided an area surrounding the signal conductor connecting conductive via that is free of the ground plane layer.

15. (Original) The printed circuit board of claim 14, wherein for each ground conductor connecting conductive via of the ground plane layer, there is provided at least one discrete area adjacent the ground conductor connecting conductive via that is free of the ground plane layer.

16. (Currently amended) The printed circuit board of claim 9, further comprising a plurality of signal conductor connecting conductive vias, each signal conductor connecting conductive via being coupled to a signal conductor conductive pad of the plurality of conductive pads and a plurality of ground conductor conductive connecting vias, each ground conductor conductive connecting via being coupled to a ground conductor conductive pad of the plurality of conductive pads; and which further comprises:

a power voltage plane layer through which at least some of the plurality of conductive vias extend; and

for each signal conductor connecting conductive via and its corresponding adjacent ground conductor connecting conductive vias extending through the power voltage plane layer, there is provided an area surrounding the conductive vias that is free of the power voltage plane layer.

17. (Original) A printed circuit board having a surface providing a mating interface to which is electrically connected an electrical connector having signal conductors and ground conductors, the printed circuit board comprising:

a plurality of stacked dielectric layers;

the mating interface including:

a plurality of conductive vias aligned in a plurality of interleaved first and second rows, the plurality of conductive vias extending through at least a portion of the plurality of dielectric layers;

the plurality of conductive vias including signal conductor connecting conductive vias and ground conductor connecting conductive vias; and

for each of the plurality of first rows, each signal conductor connecting conductive via has corresponding ground conductor connecting conductive vias adjacent either side of the signal conductor connecting conductive via so as to form a repeating pattern along the row of ground conductor connecting conductive via - signal conductor connecting conductive via - ground conductor connecting conductive via;

for each of the plurality of second rows, each signal conductor connecting conductive via has corresponding ground conductor connecting conductive vias adjacent either side of the signal conductor connecting conductive via so as to form a repeating pattern along the row of ground conductor connecting conductive via - signal conductor connecting conductive via - ground conductor connecting conductive via; and

the positions of the signal conductor connecting conductive vias in the first rows relative to the positions of the signal conductor connecting conductive vias in the second rows are offset so that each signal conductor connecting conductive via in the first and second rows has a ground conductor connecting conductive via adjacent at least three sides.

18. (Original) The printed circuit board of claim 17, wherein for each of the plurality of first and second rows of the conductive vias, a distance between a signal conductor connecting conductive via and an adjacent ground conductor connecting conductive via on one side is similar to a distance between the signal conductor connecting conductive via and an adjacent ground conductor connecting conductive via on the other side.

19. (Original) The printed circuit board of claim 17, which further comprises a surface mounting pad disposed on each of the plurality of conductive vias, the signal conductors and ground conductors of the electrical connector being electrically connected to the surface mounting pads.